UNITED STATES PATENT AND TRADEMARK OFFICE

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10/620,628	07/15/2003	John Xiaoxiong Zhong	SYN-0551CON1	1718

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN XIAOXIONG, DIAN YANG,
ZHENG ZHOU,
and
TING WANG

Appeal 2008-005123
Application 10/620,628
Technology Center 2800

Decided:[1] May 28, 2009

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY,
and CARL W. WHITEHEAD, JR., *Administrative Patent Judges.*

WHITEHEAD, JR., *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-2, 4, 6-12, 14 and 16-20. *See* App. Br. 3. We have jurisdiction under 35 U.S.C. § 6(b) (2002). We affirm.

STATEMENT OF THE CASE

Appellants invented a method for performing verification of a design by using symbolic simulation.[2]

Claim 1 which further illustrates the invention follows:

> 1. A method for performing design verification, the method comprising:
> specifying at least one hardware description language object that represents at least one signal as a symbol in a design using a first statement that is part of a hardware description language; and
> instructing a symbolic simulator in response to the first statement to treat the at least one hardware description language object as a symbol.

The Rejections

The Examiner relies upon the following prior art references as evidence of unpatentability:

Gary York et al., *An Integrated Environment for HDL Verification* Verilog HDL Conference - IEEE, 9-18 (1955) (hereinafter "York").

Charles Dawson et al., *The Verilog Procedural Interface for the Verilog Hardware Description Language*, IEEE, 17-22 (1996) (hereinafter "Dawson").

Claims 1, 2, 4, 6-8, 11, 12, 14 and 16-18 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over York (Ans. 3-5).

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[2] *See generally* App. Br. 4 and Spec 2.

Claims 9, 10, 19 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over York and Dawson (Ans. 5-7).

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2008).

Claims 1, 2, 4, 6-8, 11, 12, 14, and 16-18

Appellants argue that York's methodology requires that symbolic inputs are supplied at the start of the symbolic simulation which is contrary to the claimed invention (App. Br. 8). It is the Examiner's position that York's use of inputs and subsequent symbolic simulation discloses the claimed invention (Ans. 8-9).

ISSUE

Have the Appellants shown that the Examiner erred in finding that York discloses methodology wherein the symbolic simulator responds to a first statement to treat the hardware description language object as a symbol?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

York

1. Boolean variables are applied to the inputs of the receivers during the Verilog simulation and are simulated symbolically (section 3.3, para. 4).

PRINCIPLES OF LAW

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. Of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted) (internal quotation marks omitted). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted).

"'For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference.'" *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990) (quoting *Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 677 (Fed.Cir.1988)). "These elements must be arranged as in the claim under review," *Bond*, 910 F.2d at 832 (citing *Lindemann Maschinenfabrik v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984)), but this is not an "'ipsissimis verbis'" test, *Bond*, 910 F.2d at 832-33 (citing *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 n.11 (Fed. Cir. 1986)). "'[A]nticipation is a fact question subject to review under the clearly erroneous standard.'" *Bond*, 910 F.2d at 833 (quoting *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986)).

ANALYSIS

Appellants argue that claim 1 requires a first statement to start symbolic simulation of the hardware description language object that represents a signal as a symbol. *See* App. Br. 7. The Examiner argues that York's symbolic simulation must use a programming statement, which is equivalent to Appellants' first statement, in order to represent the inputs as symbolic expressions (Ans. 8).

In the specification, the Appellants state, "[t]he present invention allows hardware description languages that are normally used to describe designs to be used in symbolic simulators." (Spec. 10:17-18). However, claim 1 states, "at least one hardware description language object that represents at least one signal as a symbol." Claim 1 is describing a basic symbolic input signal. York discloses the employment of symbolic input signals (FF 1). Claim 1 does not describe the hardware description language object with any specificity that would distinguish it from the inputs used in the York invention. Therefore, we do not find Appellants' arguments persuasive because the arguments are not commensurate with the scope of the claims.

It is the Appellants' position that the claimed symbolic simulator treats the hardware description language object as a symbol therefore eliminating the need for the user to manually specify the signal during the simulation (App. Br. 7). The Appellants further argue that in York's methodology, the symbolic inputs must be supplied at the start of the symbolic simulation as opposed to the claimed invention where the symbolic simulator responds to a first statement to treat the hardware description language object as a symbol (App. Br. 8-9). York applies symbolic Boolean

variables to the input of receivers and simulates symbolically (FF 1). York does not specify that the input signals have to be manually labeled or manipulated as the Appellants have argued; however, it is apparent that the symbolic simulator of York is capable of treating the symbolic input signals (FF 1). Therefore, we do not find Appellants' arguments persuasive. As we previously stated, the language of claim 1 describes a symbolic input signal that is indistinguishable from York's symbolic input signal. The Appellants' "using a first statement" limitation fails to distinguish the claimed invention over the York reference because it is clear the symbolic simulator of York is programmed to treat the symbolic input signals without manual manipulation (FF 1).

Therefore, for the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of claim 1 and therefore we will sustain the Examiner's rejection of claim 1 and claims 2, 4, 6, 7, and 8 which fall with claim 1.

The Appellants argue that for substantially the same reasons as argued with respect to claim 1, claim 11 is also allowable over York (App. Br. 9). Therefore, for the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of claim 11 and therefore we will sustain the Examiner's rejection of claim 11 and claims 12, 14, 16, 17, and 18 which fall with claim 11.

Claims 9, 10, 19, and 20

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

ANALYSIS

The Appellants argue that although Dawson describes a new C-programming interface for Verilog hardware description language, Dawson fails to disclose a first statement that instructs the symbolic simulator to treat the hardware description language object as a symbol. *See* App. Br. 10.

We find that Appellants have not persuasively rebutted the Examiner's prima facie case of obviousness for claims 9, 10, 19, and 20, but merely contended that the additional references fail to cure the previously-noted deficiencies of York. Therefore, for the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of claims 9 and 10, which depend from claim 1, and claims 19 and 20, which depend from claim 11 and therefore we will sustain the Examiner's rejection of claims 9, 10, 19, and 20.

CONCLUSION

Appellants have not shown that the Examiner erred in finding that York discloses methodology wherein the symbolic simulator responds to a first statement to treat the hardware description language object as a symbol.

ORDER

We have sustained the Examiner's decision rejecting claims 1, 2, 4, 6-12, 14, and 16-20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2007).

AFFIRMED

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